REMARKS/ARGUMENTS

In response to the Office Action dated February 12, 2004, claims 1 and 5 are amended, and claims 9-20 are canceled without prejudice, waiver, or disclaimer to the subject matter contained therein. Claims 1-8 remain in the application. It is not the Applicants' intent to surrender any equivalents because of the amendments or arguments made herein. Reexamination and reconsideration of the application, as amended, are respectfully requested.

Election/Restriction

In paragraphs 1-5 of the Office Action, claims 1-20 were subject to a restriction requirement. Affirmation of the election of claims 1-8 is required in this response.

The Applicant thanks the Examiner and formally elects claims 1-8. To expedite prosecution of claims 1-8, the Applicant has formally canceled claims 9-20 without prejudice, waiver, or disclaimer to the subject matter therein, and reserves the right to file claims 9-20 in divisional applications.

Drawing Objections

In paragraph 6 of the Office Action, Figures 3A and 8A were objected to for the label "tow lines before present line."

The Applicant thanks the Examiner and has amended the typographical error in the label to read "two lines before present line." No new matter has been added.

Art-Based Rejections

In paragraphs 7-8 of the Office Action, claims 1, 2, 5, and 6 were rejected under 35 U.S.C. § 102(b) as being anticipated by Tada et al., USPN 4,893,195.

In paragraphs 9-10 of the Office Action, claims 3, 4, 7, and 8 were rejected under 35 U.S.C. § 102(b) as being unpatentable over Tada et al., USPN 4,893,195 in view of Honma et al., USPN 5,280,348.

The Applicant respectfully traverses the rejections, however, in order to expedite prosecution, the Applicants have amended the claims for clarification. The Applicants respectfully submit that the claims are patentable in light of the clarifying amendments above and the arguments below.

The Tada Reference

The Tada reference discloses an image processing apparatus capable of eliminating moiré pattern. FIG. 4 is a block diagram of the electrical reducing circuit and FIG. 5 is a time chart showing inputs and outputs of a main portion of the electrical reducing circuit of FIG. 4.

The operation will be described in the following with reference to FIG. 4 and FIG. 5. The image data D1 enters a latch circuit 44 at the timing of the clock CK1. The reducing data SN from the CPU 26 is inputted to a circuit for generating the clock CK2 comprising an adder 47, a latch circuit 48 and an AND gate 49. The adder 47 having a capacity of 1024 adds the reducing data SN to the output of the latch circuit 48 and outputs the same to the latch circuit 48. The timing of the output of the latch circuit 48 is supplied by the clock CK1.

When the result of addition by the adder 47 reaches 1024, a carry signal is sent to the AND gate 49. The AND output of the carry signal and the clock CK1 becomes the clock CK2. The latch circuit 44 latches the image data D1 by the clock CK2 and holds the data until the next clock CK2 is inputted. Therefore, the image data D1 entering the latch circuit 44 at the timing of the clock CK1 before the next clock CK2 is inputted will be discarded.

The image data outputted from the latch circuit 44 at the timing of the clock CK2 is written in a line RAM 45 having a storage capacity of 1 line. The clock CK2 is also inputted to the address counter 46 of the line RAM 45, whereby the data of reduced images which is thinned out in accordance with a prescribed manner (CK2 - CK1) is written in successive address locations in the line RAM 45. In this embodiment, the reducing magnification rate (1/N) is represented by 10 bits, and the magnification rate can be set as multiples of 1/1024. FIG. 5 shows a timing chart of the electrical reducing circuit 16 with the moire pattern eliminating magnification rate Nd designated as 1.5. The reducing data signal SN is set to 683 and the output of the clock CK2 is obtained as follows. The reference characters x and y denote addition data shown in FIG. 4 and characters "a" to "g" correspond to output pulses of the clock CK1 shown in FIG. 5. See Col. 6, lines 10-67.

The Honma Reference

The Honma reference discloses a color image processing apparatus.

FIG. 13 shows an example of a magnification-change control circuit for a magnification change in the main scanning direction, provided with address counters 480, 483 for supplying the memory 77 respectively with a write address and a read address, by counting the pixel transfer clock signal VCLK or a reduced-

rate clock signal CKa. A binary rate multiplier 482 generates said reduced-rate clock signal CKa by eliminating a part of the clock signal VCLK at a rate determined by a set signal SET8 as shown in FIG. 14A. As an example, for a set signal SET8 of 8 bits (2^8 =256), an output frequency f.sub.out is given by a following equation, as a function of the input frequency f_{in}:

f_{out} =M/256.f_{in}

wherein M is a value set by the signal SET8.

In the example shown in FIG. 14A, M is set as 192, so that the output frequency f_{out} is reduced to 3/4 of the input frequency f_{in}.

The magnification change is achieved by supplying said reduced clock signal CKa and the input clock signal VLCK (CKb) to a clock generating selector 407 of the address counters 405, 406. A desired magnification change can be achieved by selecting the clock signals CKa, CKb in combinations shown in FIG. 14B. Also a continuous magnification change is rendered possible by continuously varying the value M of the set signal SET8. See Col. 9, line 45-Col. 10, line 5.

The Claims are Patentable over the Cited Reference

The claims of the present invention describe an image processing method for providing interpolation processing of pixel data. A method in accordance with the present invention comprises keeping a final enumerated value of the counter for a former unit instead of resetting the final enumerated value, while still resetting a latch circuit at the end of the former unit, and carrying out a counting processing at a beginning of a current unit with a consecutive enumerated value from the kept final enumerated value.

The cited references do not teach nor suggest the limitations of the claims of the present invention. Specifically, the cited references do not teach nor suggest at least the limitation of keeping a final enumerated value of the counter for a former unit instead of resetting the final enumerated value, while still resetting a latch circuit at the end of the former unit as recited in the claims of the present invention.

The Tada reference merely thins out the clock signal to reduce one line of pixel data in a main scanning direction with the adder 47 and the latch circuit 48. The adder 47 adds the reducing data SN to the output of the latch circuit 48 and outputs that back to the latch circuit 48. See Col. 6, lines 17-27.

The present invention keeps the final enumerated value and still resets the latch circuit at the end of the former unit. If the system of Tada were to do this, the value of data coming from the latch circuit 48, which would be zero, would provide nothing to add to the reducing data SN as described above. Thus, the Tada reference does not teach nor suggest at least the limitation of keeping a final enumerated value of the counter for a former unit instead of resetting the final enumerated value, while still resetting a latch circuit at the end of the former unit as recited in the claims of the present invention.

The ancillary Honma reference does not remedy the deficiencies of the Tada reference; namely, neither the Honma nor the Tada reference, alone or in any combination, teach nor suggest at least the limitation of keeping a final enumerated value of the counter for a former unit instead of resetting the final enumerated value, while still resetting a latch circuit at the end of the former unit as recited in the claims of the present invention.

Thus, it is submitted that independent claims 1 and 5 are patentable over the cited reference. Claims 2-4 and 6-8 are also patentable over the cited references, not only because they contain all of the limitations of the independent claims, but because claims 2-4 and 6-8 also describe additional novel elements and features that are not described in the prior art.

Conclusion

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6742 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
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